

Figure 1

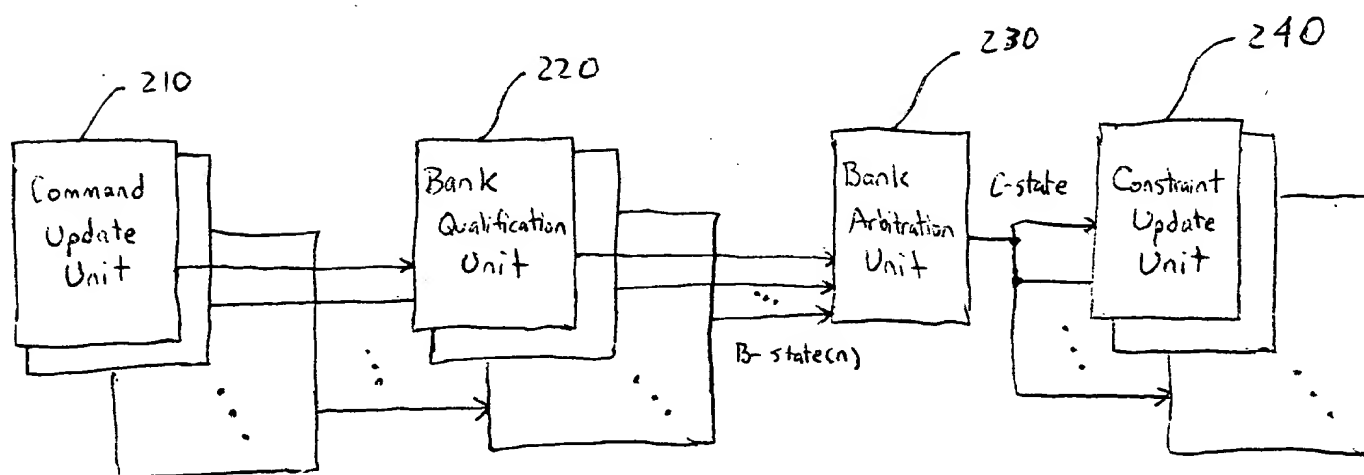


Figure 2

fig 1

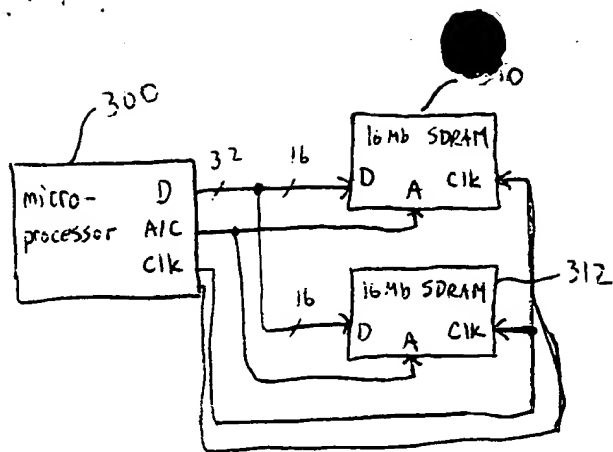


Figure 3(a)

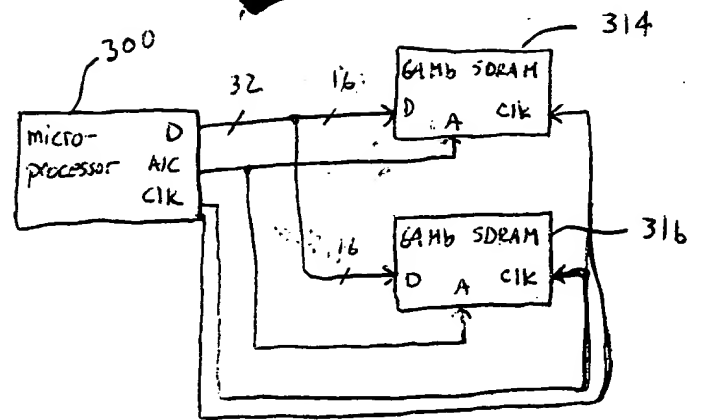


Figure 3(b)

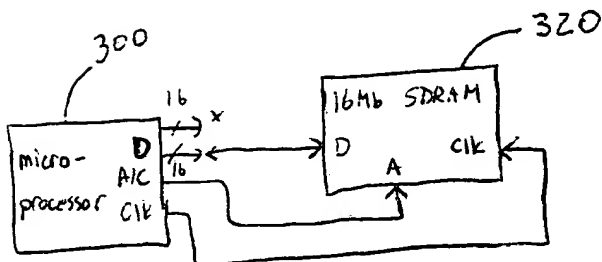


Figure 3(c)

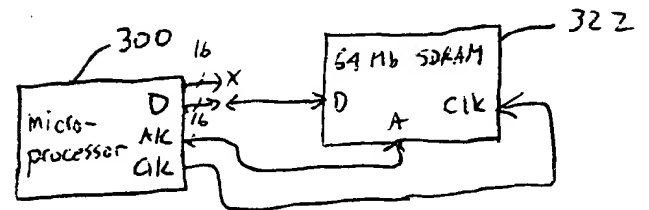


Figure 3(d)

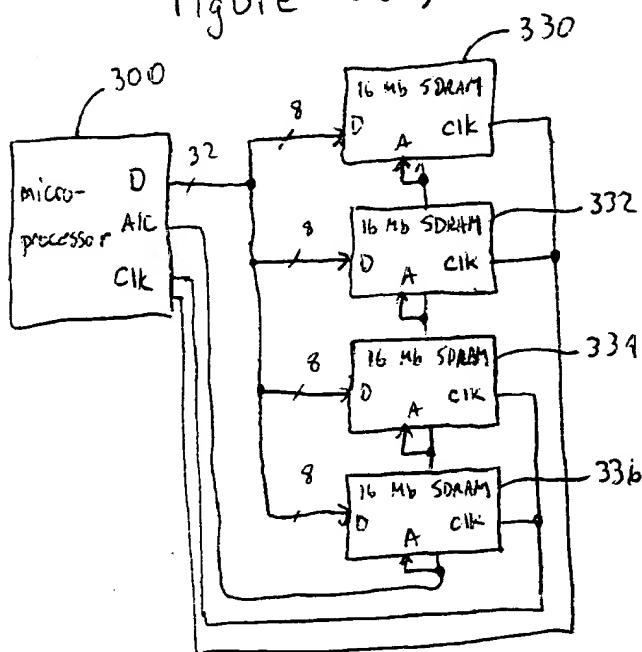


Figure 3(e)

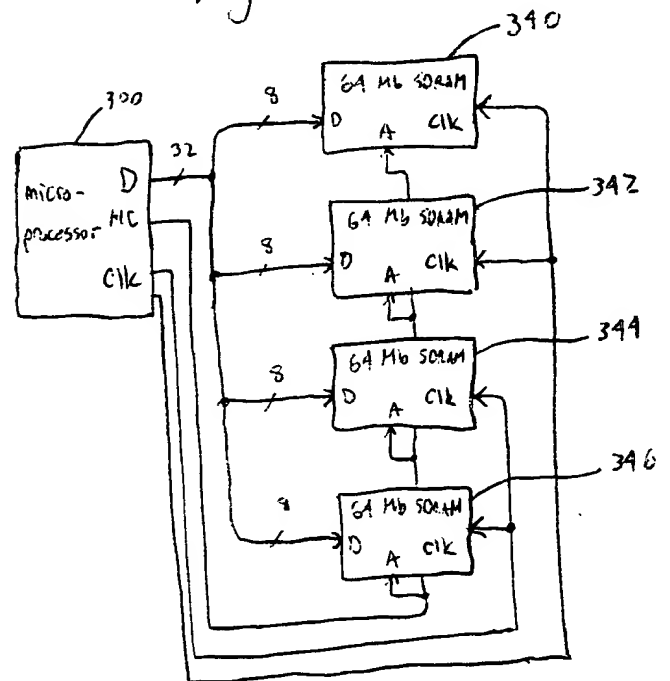


Figure 3(f)

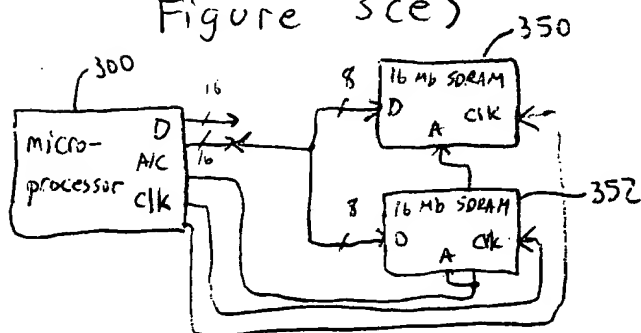


Figure 3(g)

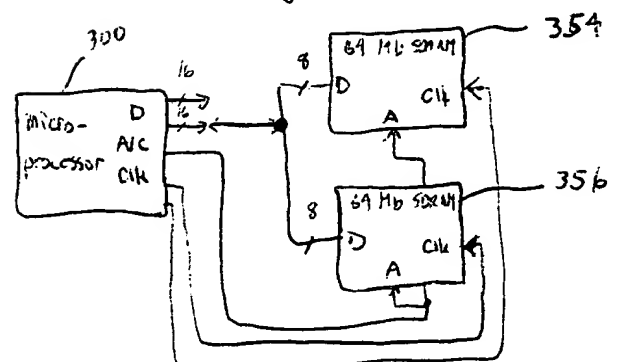
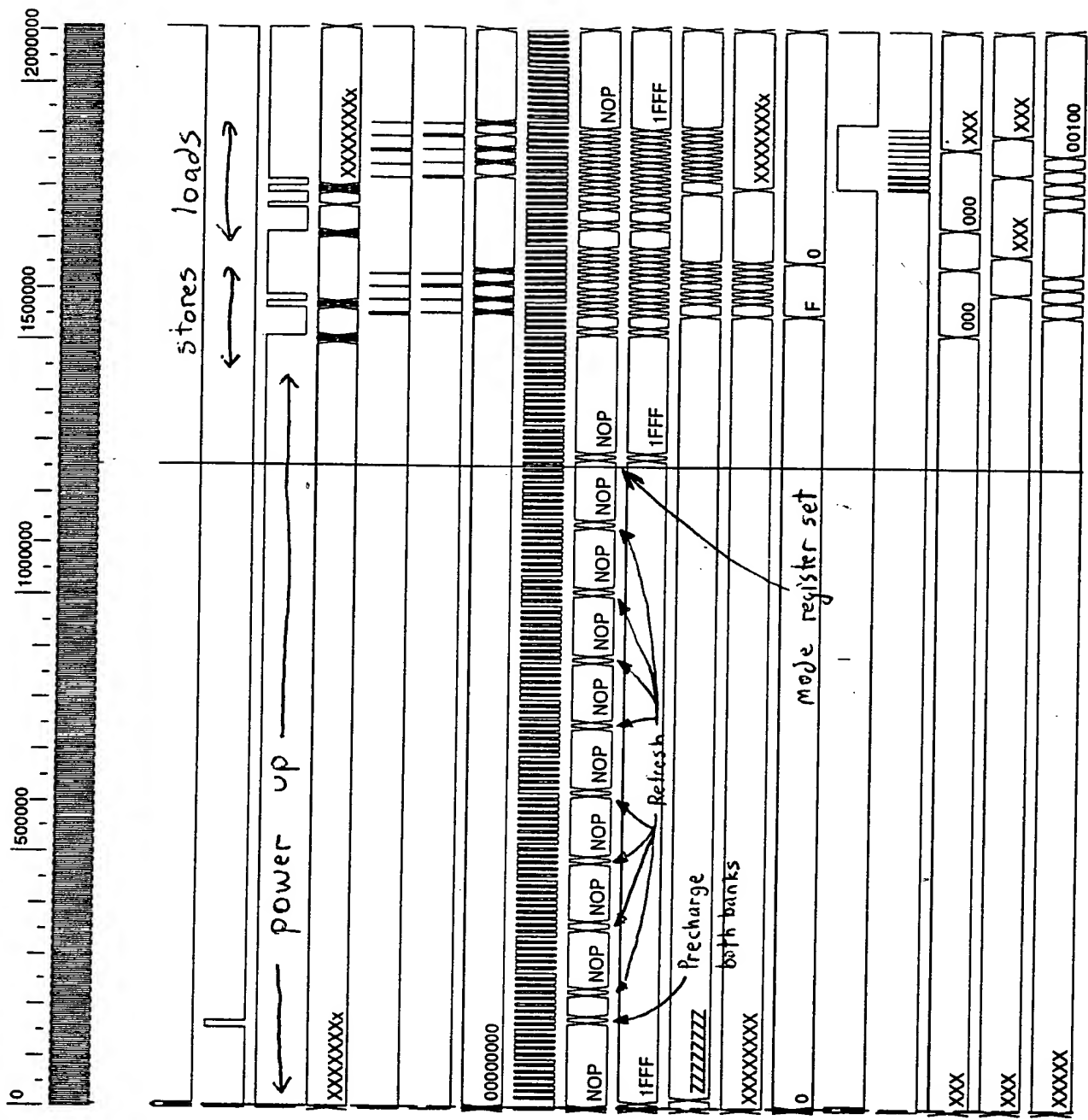


Figure 3(h)



time →

Figure 4(a)

STORES

controller Clock

Reset

Restart go

Ready

Controller Input bus

Controller Return bus Request

Controller Return bus Grant

Controller Return bus

SDRAM clock

Command

Address

Data

Output pad

Drive

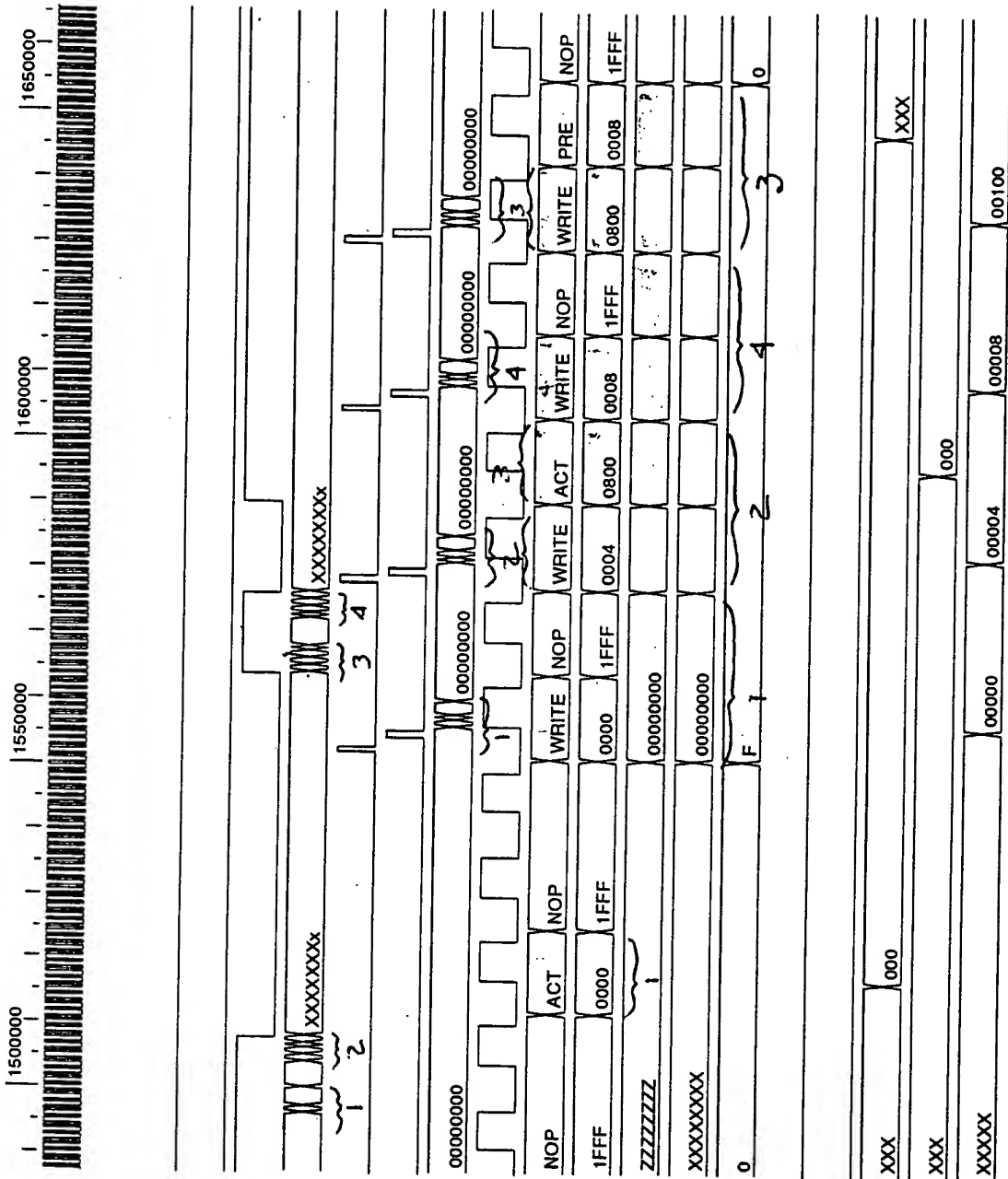
Read Window

Sample

Active Row0

Active Row1

Word Address

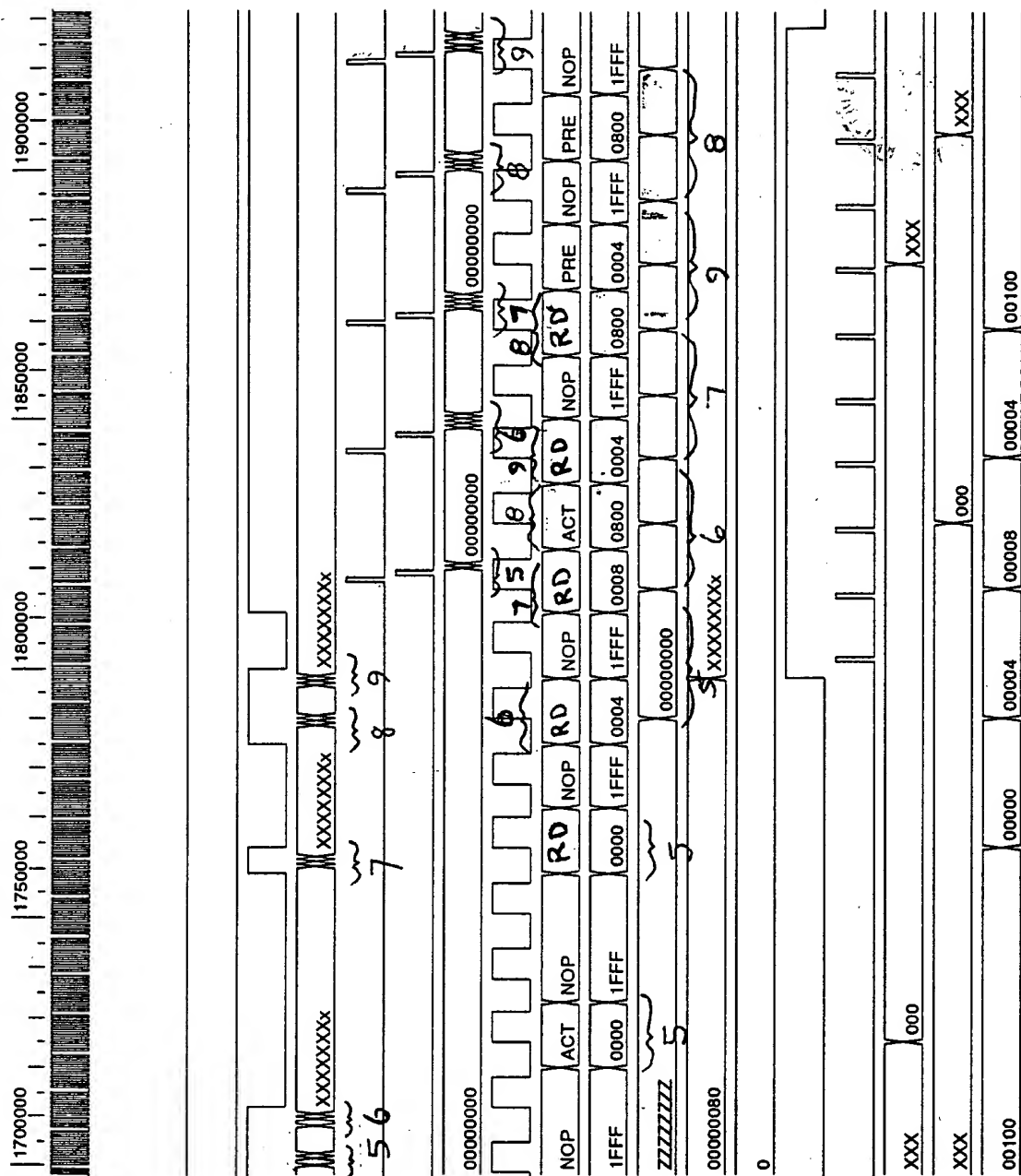


Time →

Figure 4(b)

Controller clock

- Reset
- Restart go
- Ready
- Controller Input bus
- Controller Return bus Request
- Controller Return bus Grant
- Controller return bus
- SDRAM clock
- Command
- Address
- Data
- Output to pad
- Drive
- Read window
- Sample
- Active Row 0
- Active Row 1
- Word Address



time ↑

Figure 4(c)